FIG. 1

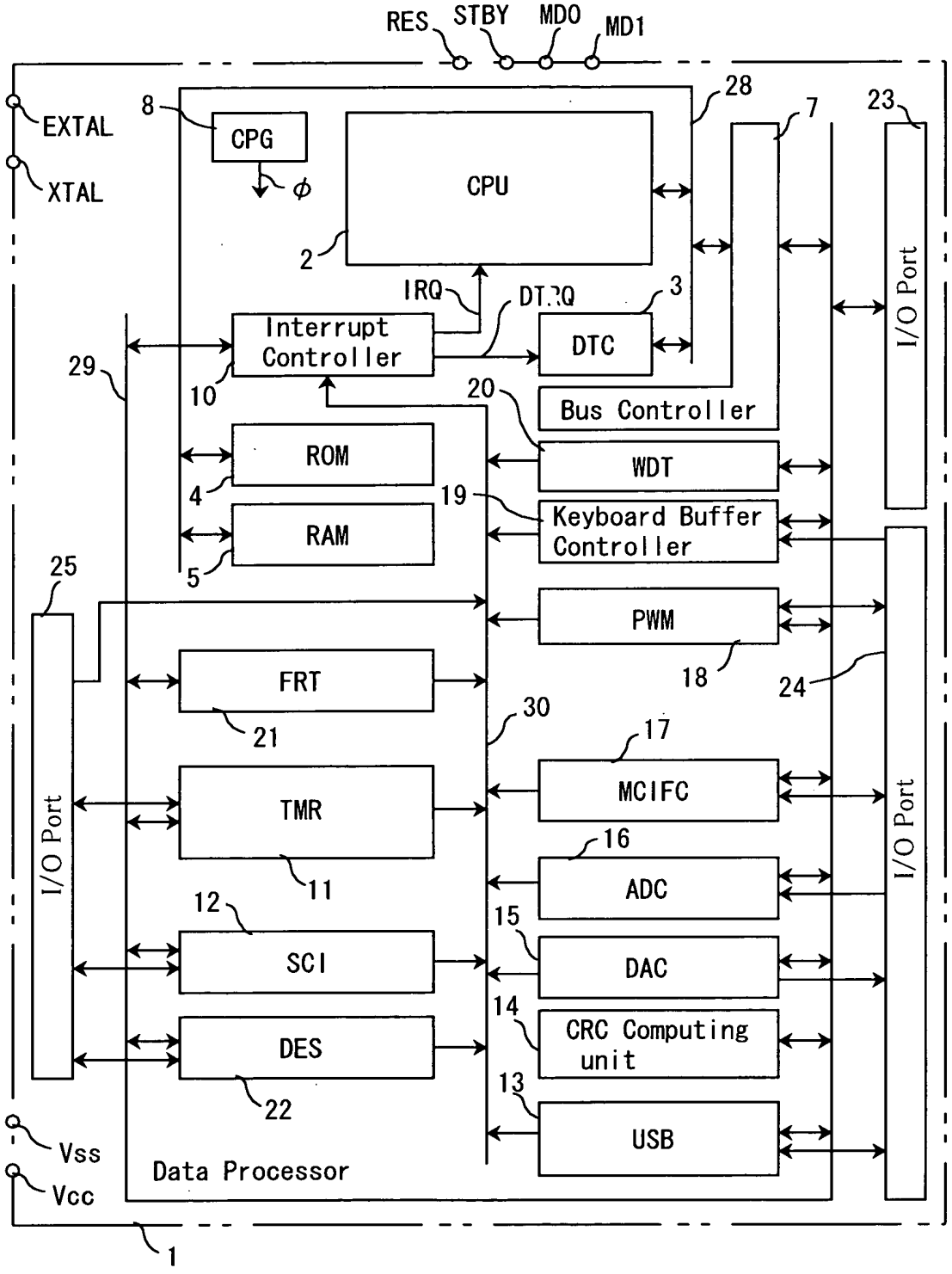

RES
STBY
MD0
MD1
EXTAL
XTAL
8
CPG
φ
CPU
2
28
7
23
I/O Port
IRQ
DTCQ
3
DTC
Interrupt Controller
10
29
20
Bus Controller
ROM
4
WDT
19
Keyboard Buffer Controller
RAM
5
25
PWM
18
24
FRT
21
30
17
MCIFC
TMR
11
16
ADC
12
15
SCI
DAC
14
CRC Computing unit
DES
22
13
USB
Vss
Vcc
Data Processor
1

FIG. 2

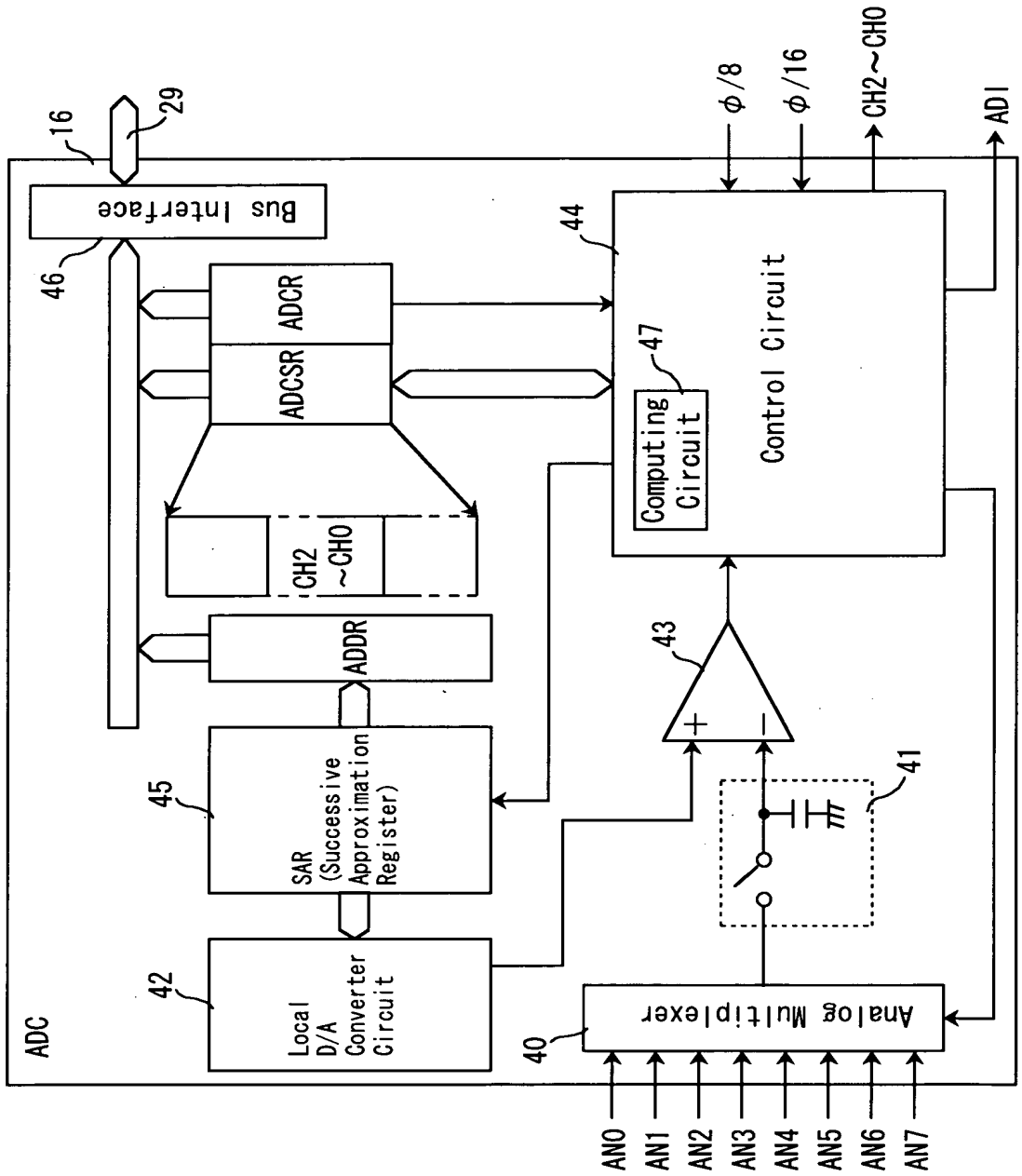

ADC
Bus Interface
16
29
46
ADCR
ADCSR
CH2 ~CH0
ADDR
45
SAR (Successive Approximation Register)
42
Local D/A Converter Circuit
44
Control Circuit
47
Computing Circuit
43
41
40
Analog Multiplexer
AN0
AN1
AN2
AN3
AN4
AN5
AN6
AN7
φ/8
φ/16
CH2~CH0
AD1

FIG. 3

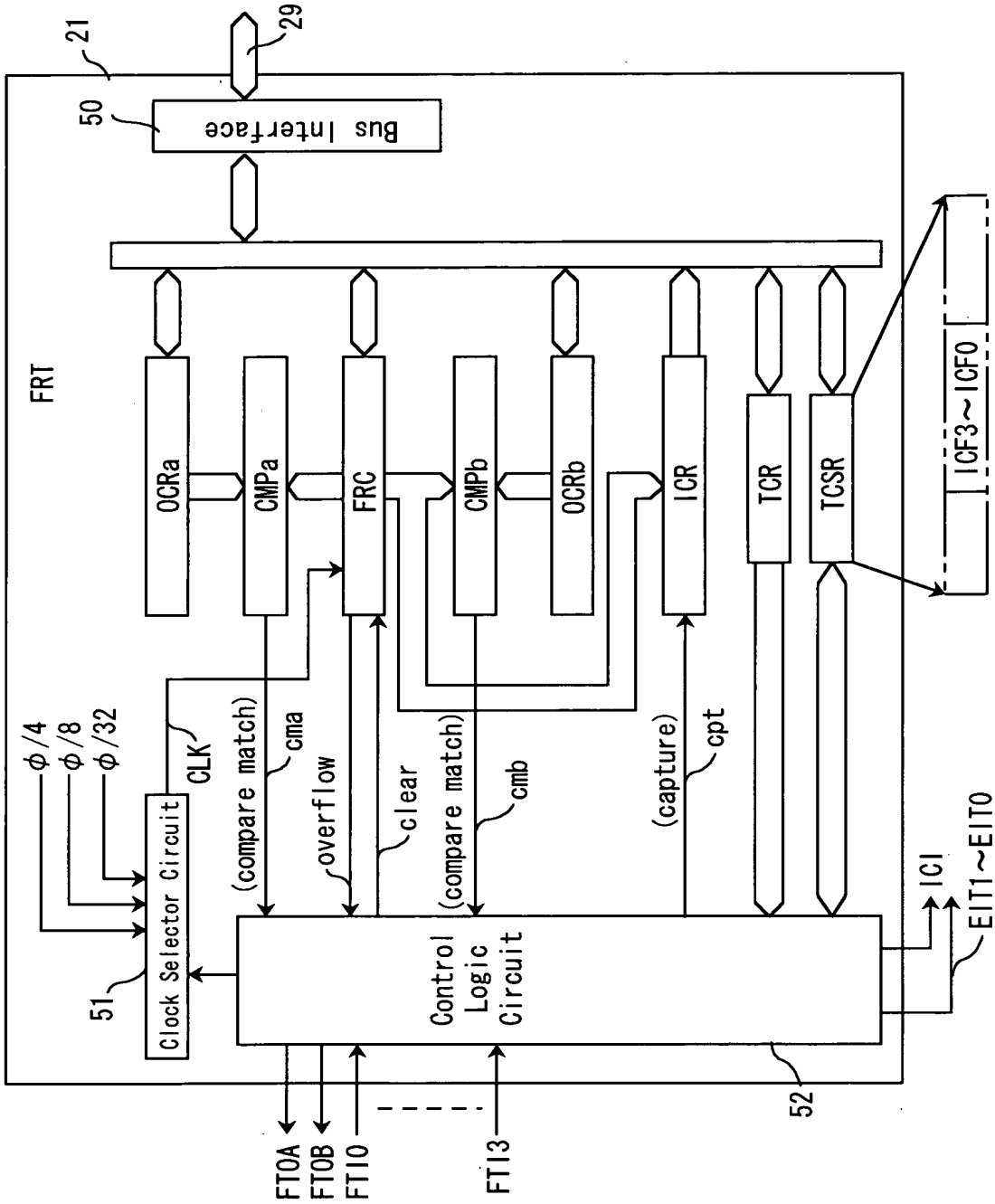

21
29
50
Bus Interface
FRT
OCRa
CMPa
FRC
CMPb
OCRb
ICR
TCR
TCSR
ICF3~ICF0
φ/4
φ/8
φ/32
CLK
(compare match)
cma
overflow
clear
(compare match)
cmb
(capture)
cpt
Clock Selector Circuit
51
Control Logic Circuit
52
ICI
EIT1~EIT0
FTOA
FTOB
FTI0
FTI3

FIG. 4

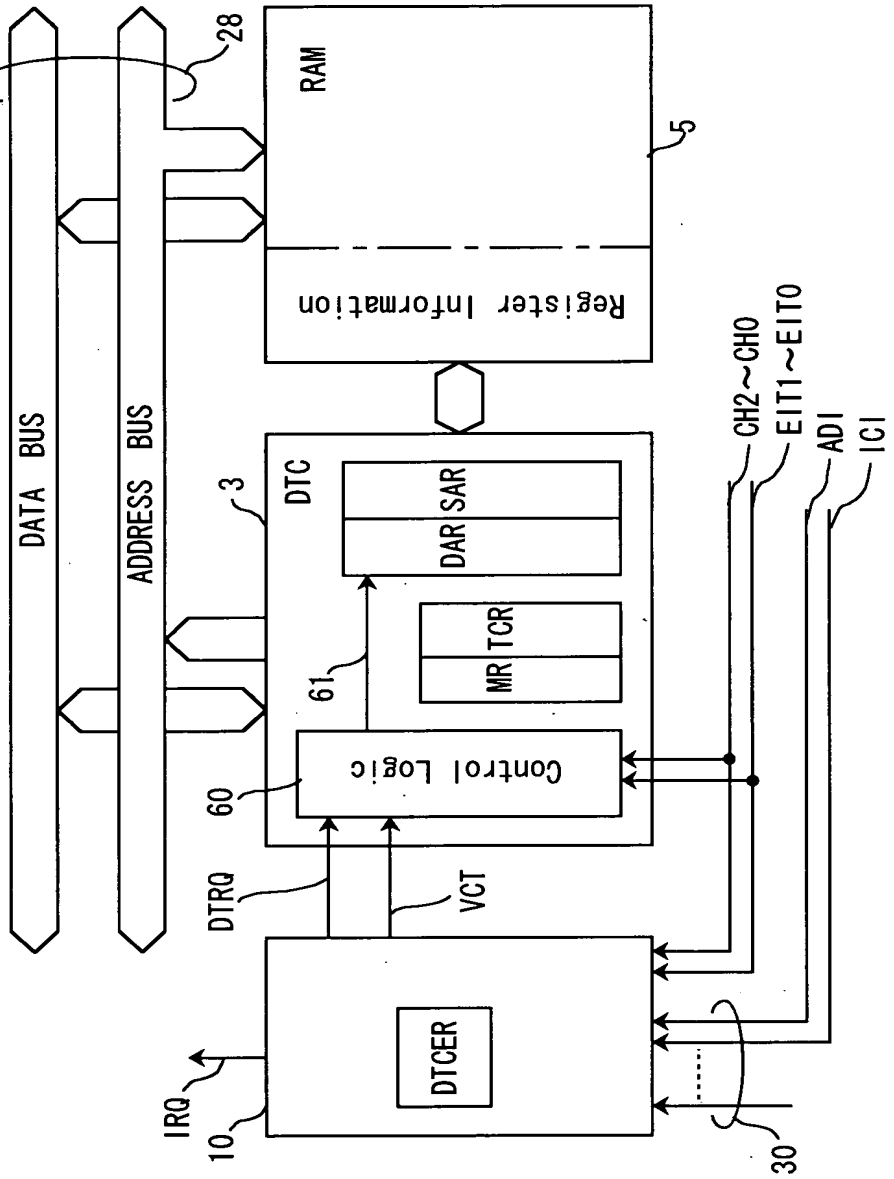

DATA BUS
ADDRESS BUS
28
RAM
5
Register Information
3
DTC
DAR SAR
MR TCR
61
Control Logic
60
DTRQ
VCT
DTCER
IRQ
10
30
CH2~CH0
EIT1~EIT0
ADI
ICI

FIG. 5

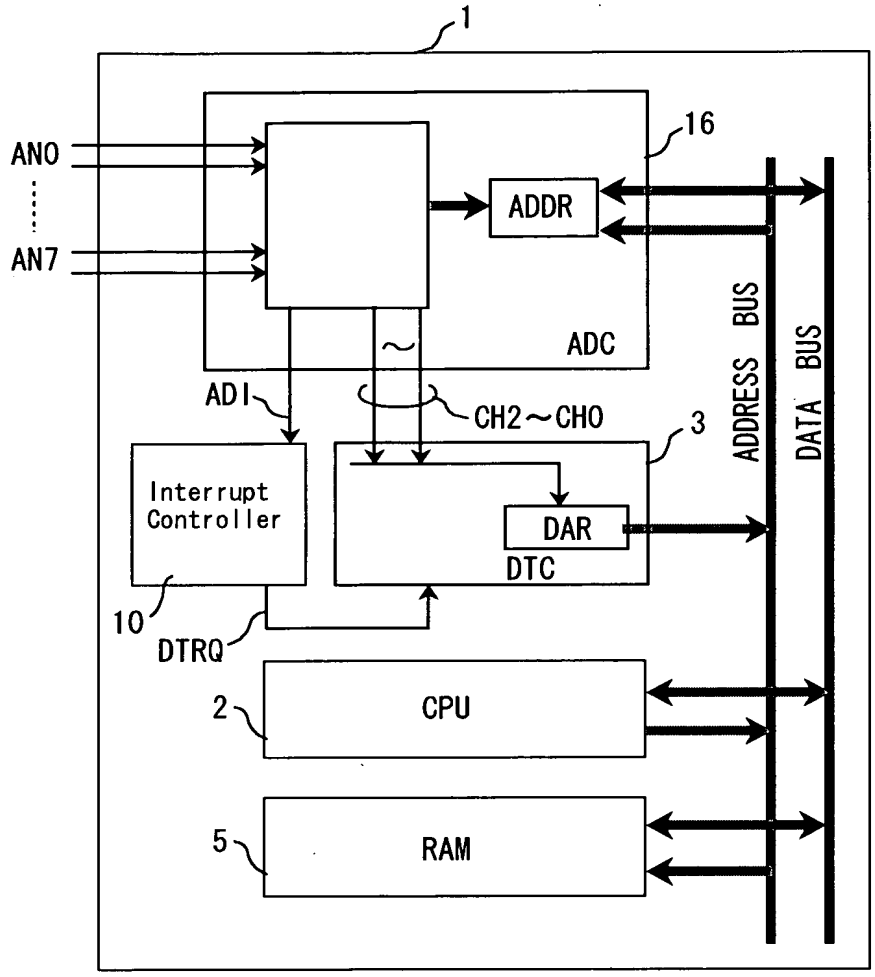

1
16
AN0
AN7
ADDR
ADC
ADI
CH2~CH0
3
Interrupt Controller
DAR
DTC
10
DTRQ
2
CPU
5
RAM
ADDRESS BUS
DATA BUS

FIG. 6

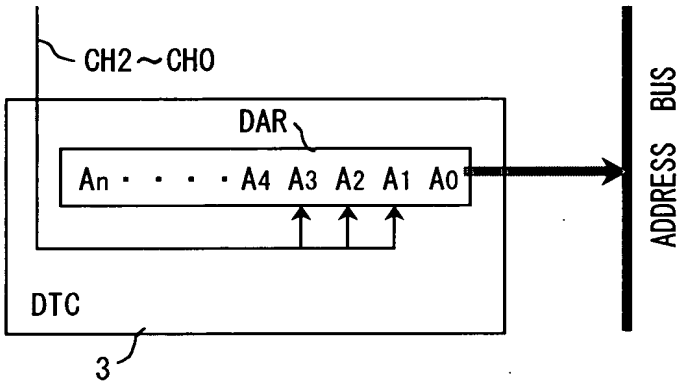


FIG. 7

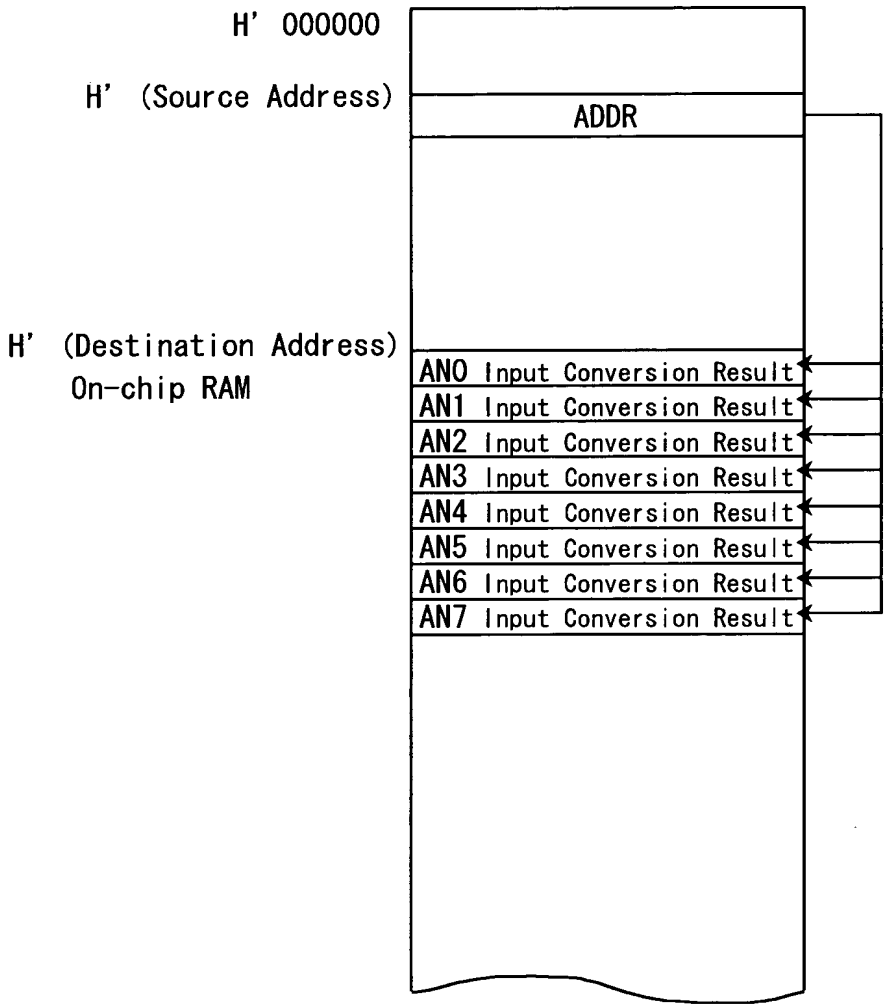

H' 000000
H' (Source Address)
ADDR
H' (Destination Address)
On-chip RAM
AN0 Input Conversion Result
AN1 Input Conversion Result
AN2 Input Conversion Result
AN3 Input Conversion Result
AN4 Input Conversion Result
AN5 Input Conversion Result
AN6 Input Conversion Result
AN7 Input Conversion Result
Address Space

FIG. 8

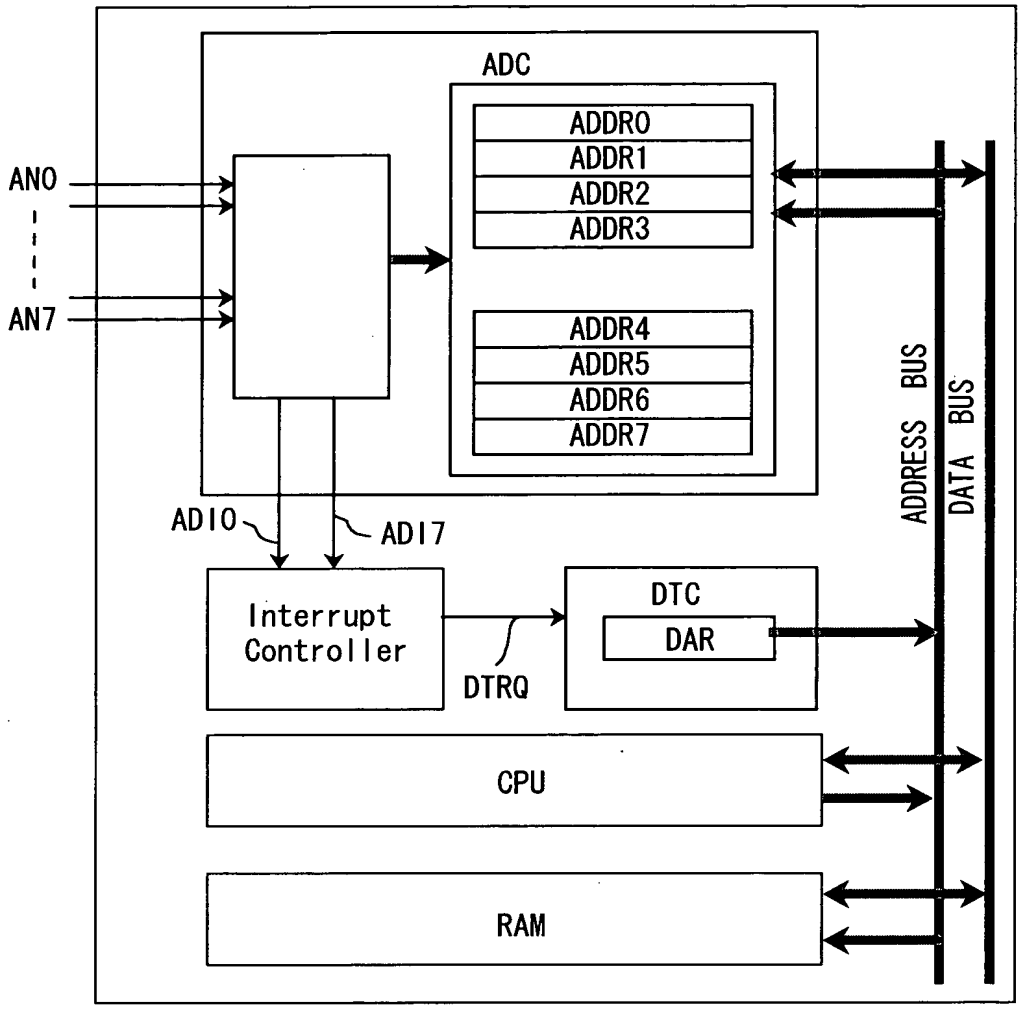

ADC
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
ADDR7
AN0
AN7
AD10
AD17
Interrupt Controller
DTRQ
DTC
DAR
CPU
RAM
ADDRESS BUS
DATA BUS

FIG. 9

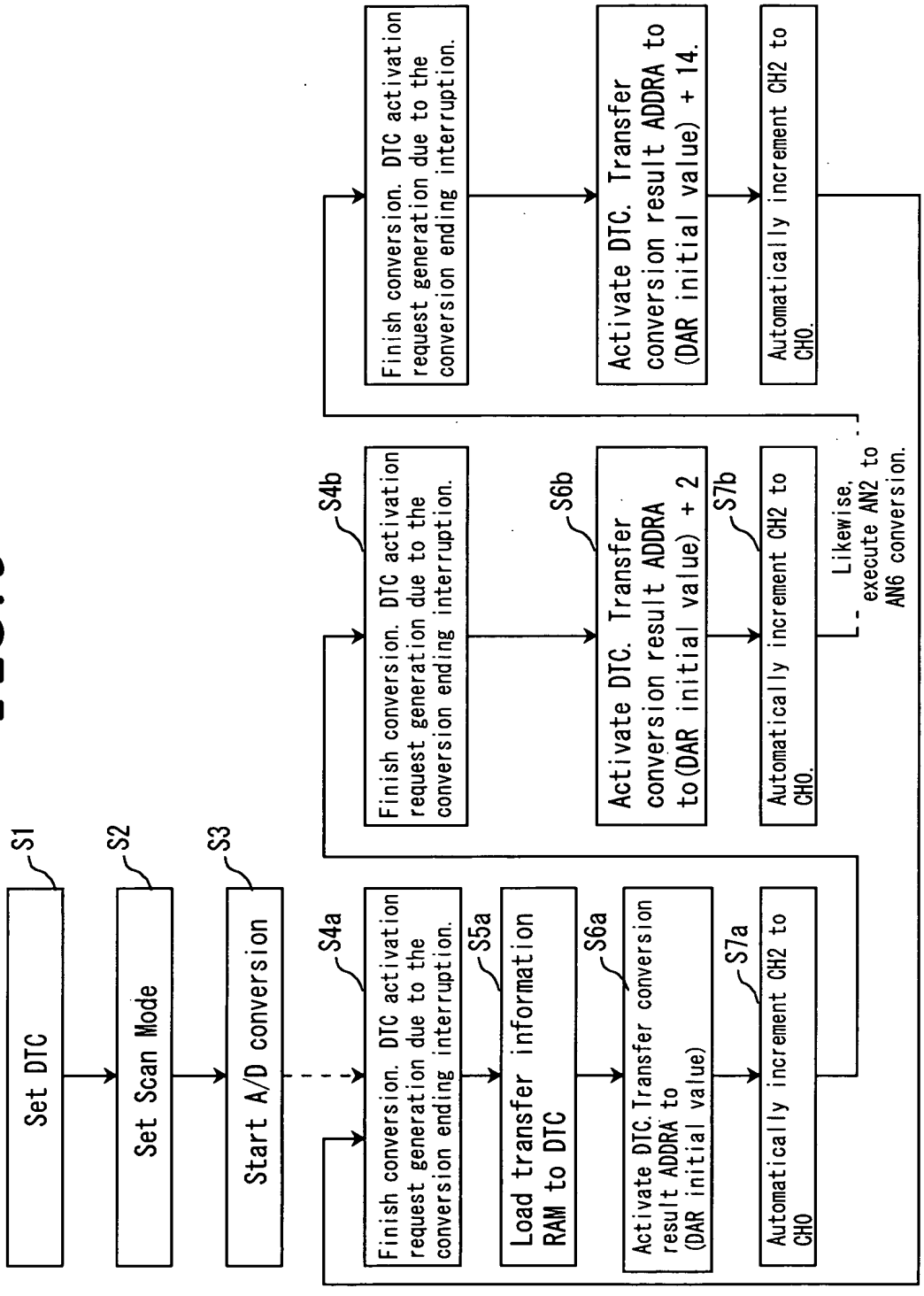

S1
Set DTC
S2
Set Scan Mode
S3
Start A/D conversion
S4a
Finish conversion. DTC activation request generation due to the conversion ending interruption.
S5a
Load transfer information RAM to DTC
S6a
Activate DTC. Transfer conversion result ADDRA to (DAR initial value)
S7a
Automatically increment CH2 to CH0
S4b
Finish conversion. DTC activation request generation due to the conversion ending interruption.
S6b
Activate DTC. Transfer conversion result ADDRA to (DAR initial value) + 2
S7b
Automatically increment CH2 to CH0.
Likewise, execute AN2 to AN6 conversion.
Finish conversion. DTC activation request generation due to the conversion ending interruption.
Activate DTC. Transfer conversion result ADDRA to (DAR initial value) + 14.
Automatically increment CH2 to CH0.

FIG.10

CH2	CH1	CH0	DAR				A/D conversion
			A3	A2	A1	A0	
0	0	0	0	0	0	0	AN0 Input Conversion
0	0	1	0	0	1	0	AN1 Input Conversion
0	1	0	0	1	0	0	AN2 Input Conversion
0	1	1	0	1	1	0	AN3 Input Conversion
1	0	0	1	0	0	0	AN4 Input Conversion
1	0	1	1	0	1	0	AN5 Input Conversion
1	1	0	1	1	0	0	AN6 Input Conversion
1	1	1	1	1	1	0	AN7 Input Conversion

FIG. 11

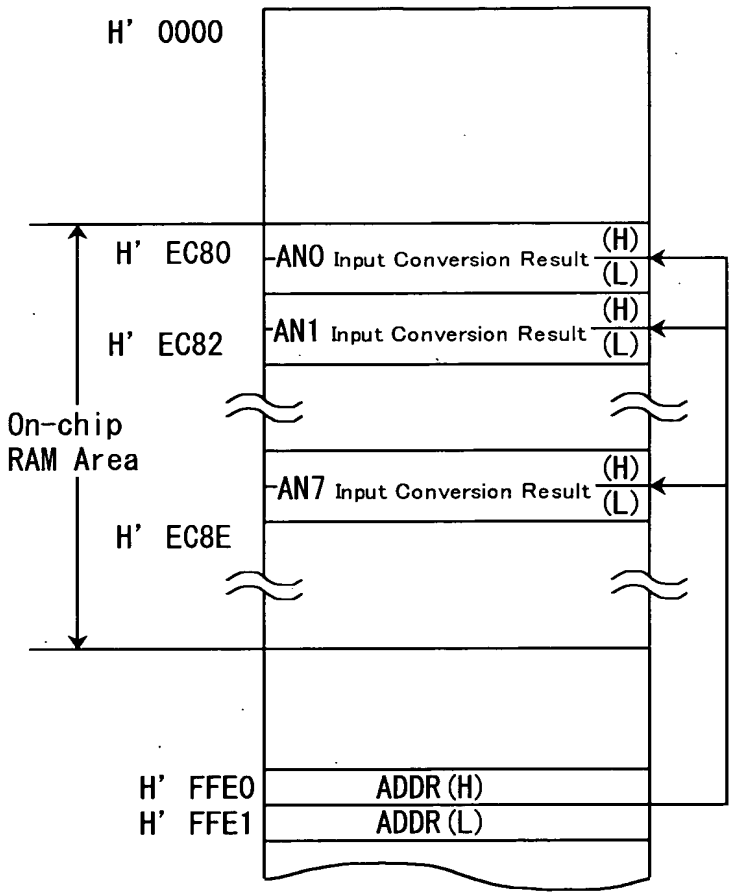

H' 0000
H' EC80
AN0 Input Conversion Result
(H)
(L)
H' EC82
AN1 Input Conversion Result
(H)
(L)
On-chip
RAM Area
AN7 Input Conversion Result
(H)
(L)
H' EC8E
H' FFE0
ADDR (H)
H' FFE1
ADDR (L)

FIG. 12

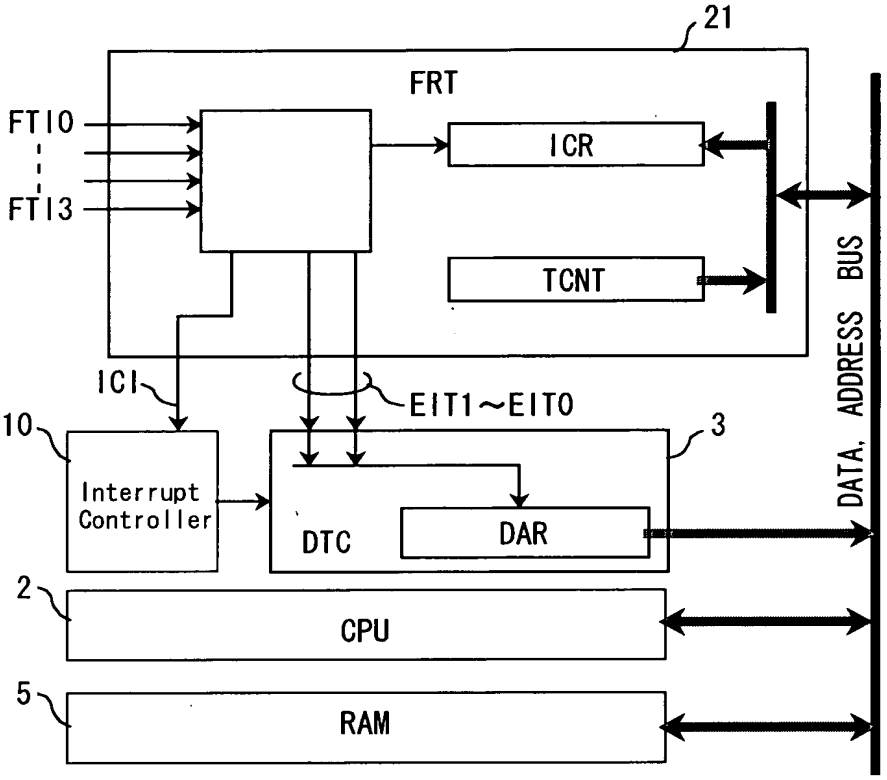

21
FRT
FTI0
FTI3
ICR
TCNT
ICI
EIT1~EIT0
10
Interrupt Controller
3
DTC
DAR
DATA, ADDRESS BUS
2
CPU
5
RAM

FIG.13

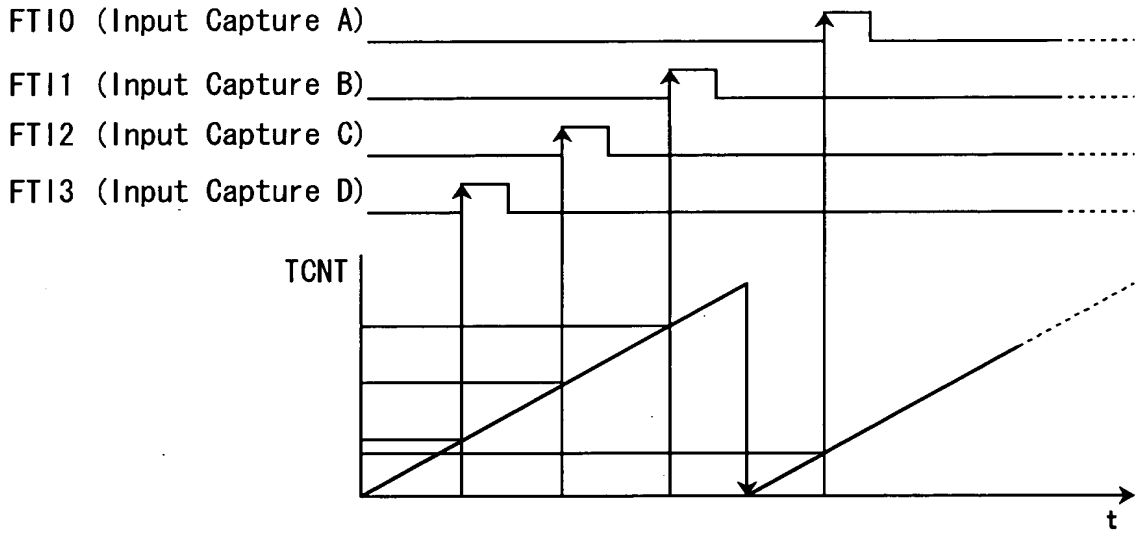

FTIO (Input Capture A)
FTI1 (Input Capture B)
FTI2 (Input Capture C)
FTI3 (Input Capture D)
TCNT
t

FIG.14

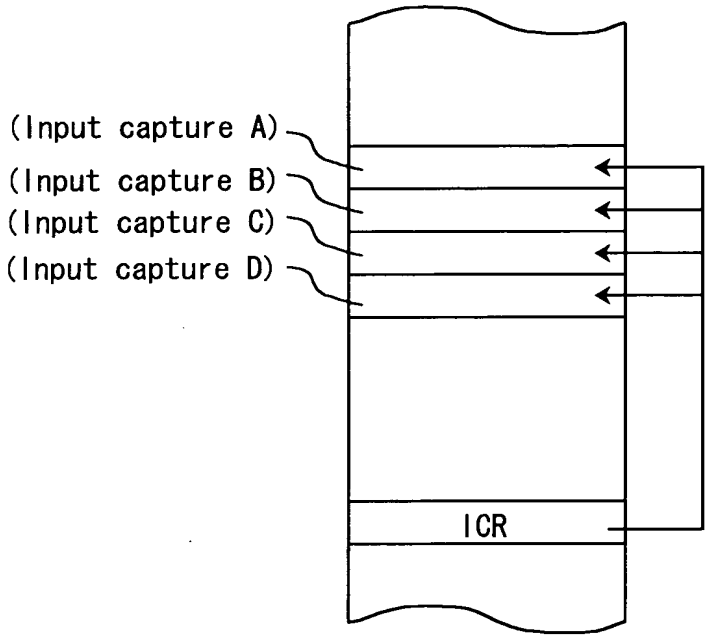

(Input capture A)
(Input capture B)
(Input capture C)
(Input capture D)
ICR

FIG. 15

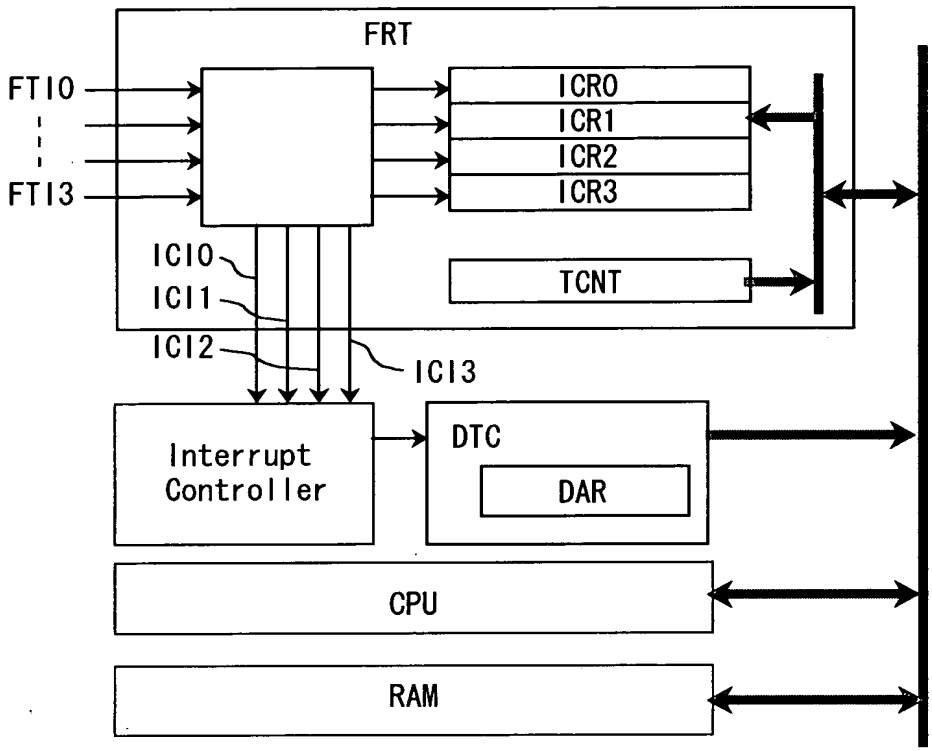

FRT
FTI0
FTI3
ICR0
ICR1
ICR2
ICR3
TCNT
ICI0
ICI1
ICI2
ICI3
Interrupt Controller
DTC
DAR
CPU
RAM

FIG. 16

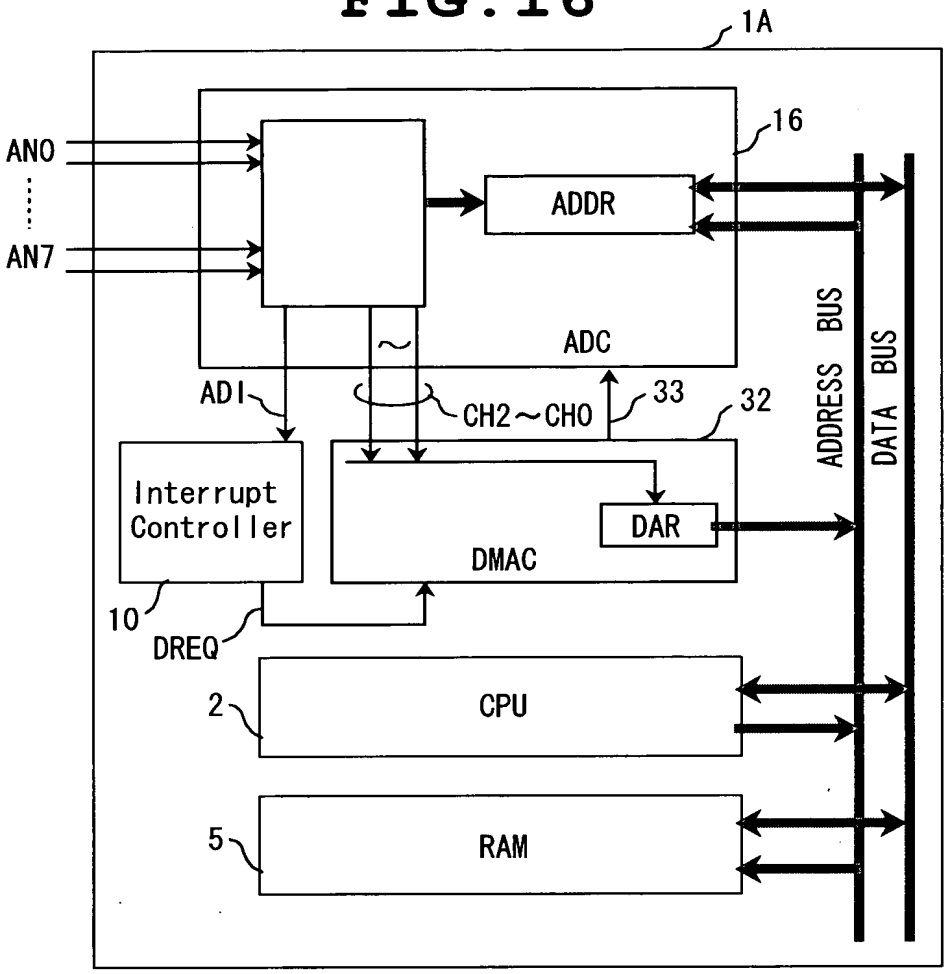

1A
16
AN0
AN7
ADDR
ADC
ADI
CH2~CH0
33
32
Interrupt Controller
DAR
DMAC
10
DREQ
2
CPU
5
RAM
ADDRESS BUS
DATA BUS

FIG.17

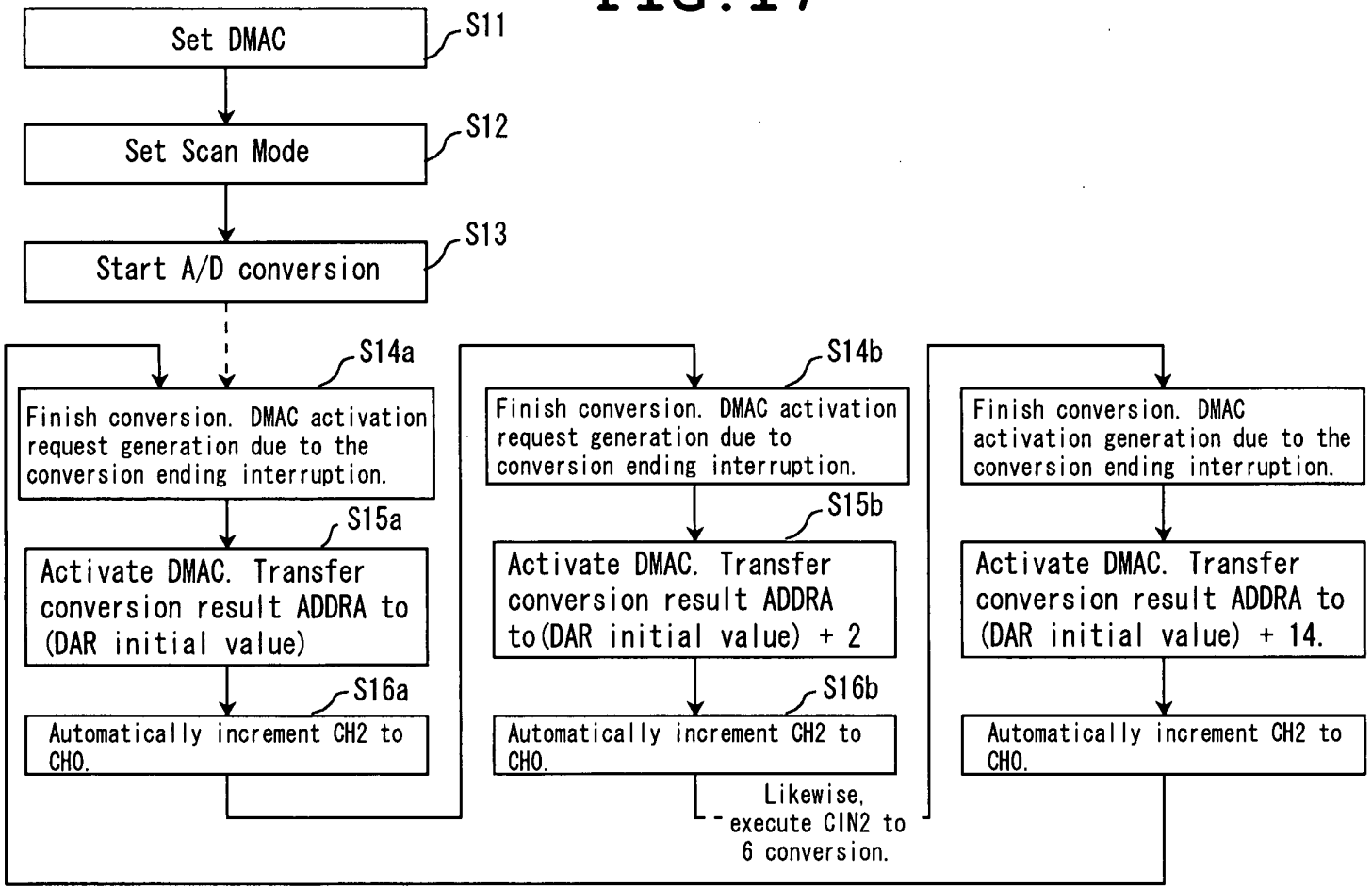


FIG. 18

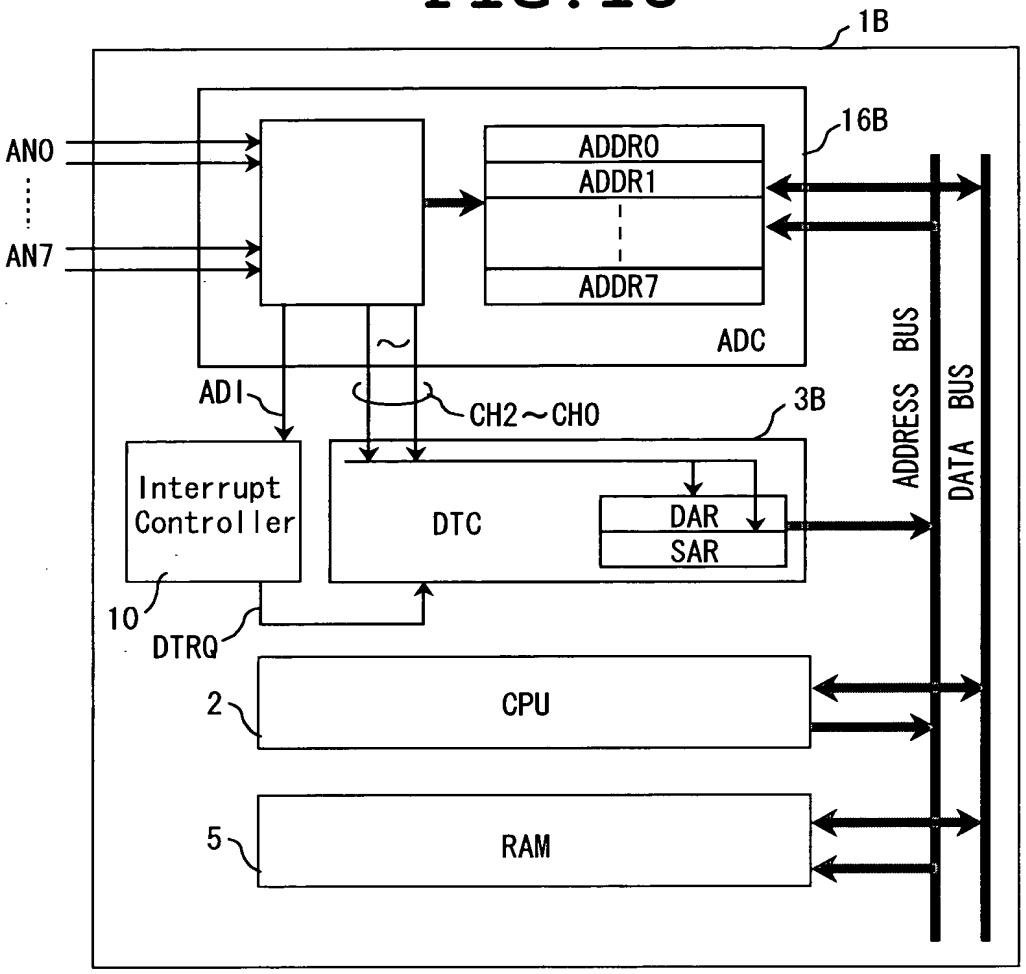

1B
16B
AN0
AN7
ADDR0
ADDR1
ADDR7
ADC
ADI
CH2~CH0
3B
Interrupt Controller
DTC
DAR
SAR
ADDRESS BUS
DATA BUS
10
DTRQ
2
CPU
5
RAM

FIG.19

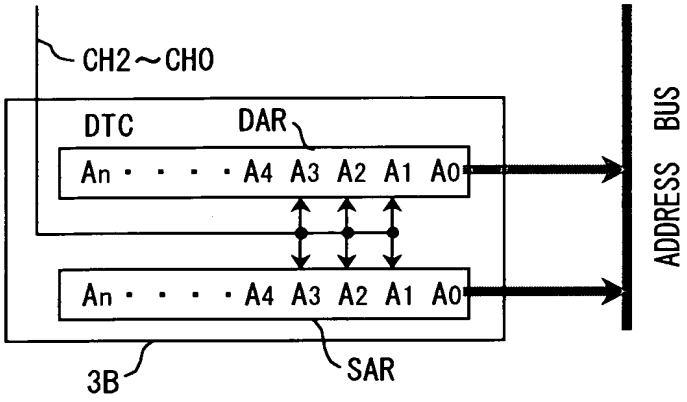

CH2~CH0
DTC
DAR
An · · · · A4 A3 A2 A1 A0
An · · · · A4 A3 A2 A1 A0
ADDRESS BUS
3B
SAR

FIG.20

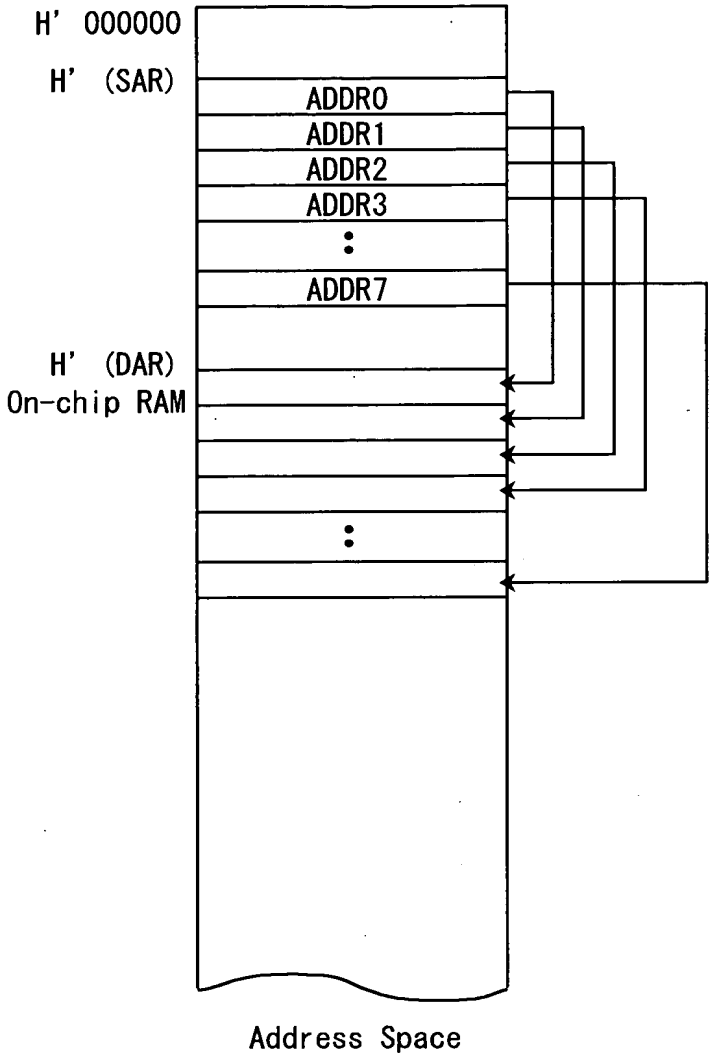
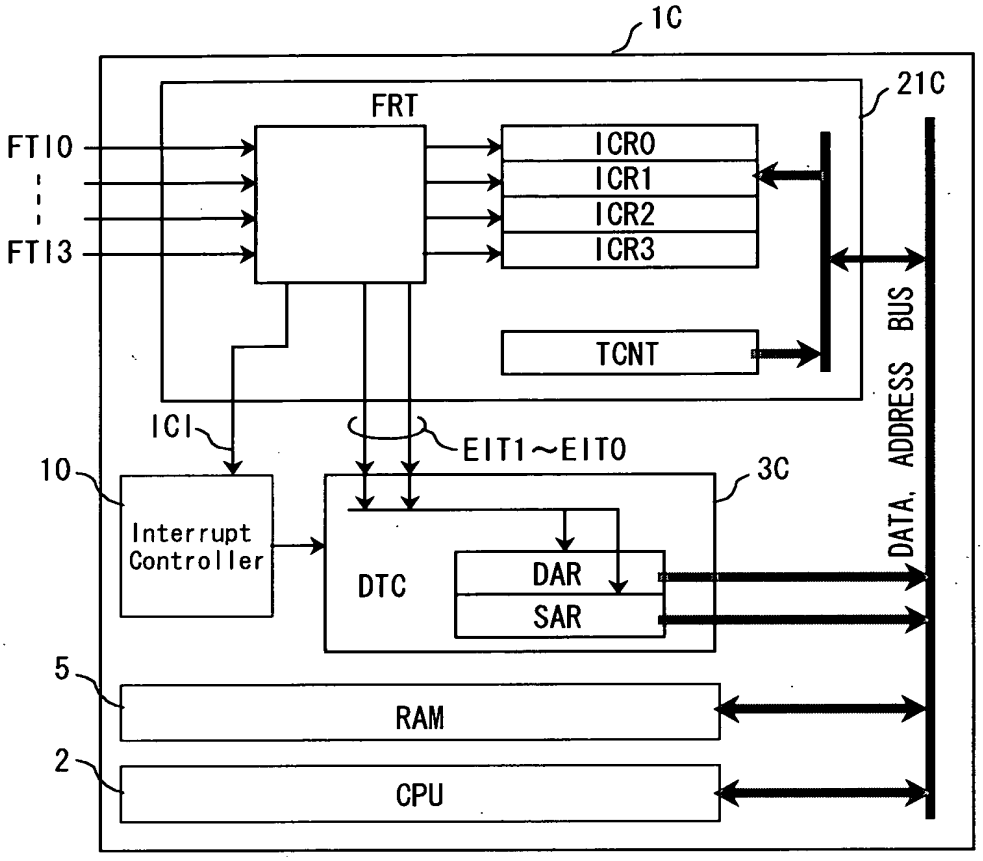

H' 000000
H' (SAR)
ADDR0
ADDR1
ADDR2
ADDR3
ADDR7
H' (DAR)
On-chip RAM
Address Space

FIG. 21


1C
21C
FRT
FTI0
FTI3
ICR0
ICR1
ICR2
ICR3
TCNT
ADDRESS BUS
DATA
ICI
EIT1~EIT0
10
3C
Interrupt Controller
DTC
DAR
SAR
5
RAM
2
CPU